

Power Rails	<Pwr Rail Name>	<Signals>	
PDN base		Control Signals: General ctrl't & logic (<i>Italic = SW config'd after boot</i>) PDN base ctrl't	<ul style="list-style-type: none"> Note items
MCU Only/Island			
Partial IO Retention (aka GPIO Ret)			<ul style="list-style-type: none"> On-Chip "Pwr OK" Monitors (OV & UV)
DDR_Retention (aka S2R)			
End Product option		Func Safety	<ul style="list-style-type: none"> On-Chip "Pwr OK" Monitors (UV only)
Peripheral loads (SW config'd after boot)		GPIO Retention	
		DDR_Retention (aka S2R)	
		End Product option	
		Peripheral compo.	
			<ul style="list-style-type: none"> Provisioned In-Line Supply Filter
			High-lighted diagram changes

ASIL-B Functional Safety (FuSa) requires voltage monitoring (VMON) of all “safety critical” power rails (i.e. key SoC supplies) that could cause severe system failures. This classification depends on the end product use case & system resources a customer is using that can impact power safety. The PMIC & SoC have internal OV & VM monitoring for key SoC input supply voltages. The status is reported by each device’s internal registers (i.e. SoC’s Power OK (POK) status bits). PMIC & SoC VMON inputs (i.e. PMIC’s VMONx, SoC’s VMONx_IR_VEXTxx) can be used to extend VMON to a few board level power rails (i.e. HPCBS built vDD_CORE, load switch’s vDD_L0_3V3). The following SoC & 3DRM supplies can be considered non-critical wrt FuSa & typically do not require direct OV/VM monitoring: VDDHVSx (SD CARD), VPP, VDDA_33V & VDD1_LPD0R4_1V8.

A) Keeping key IO & DDR supplies energized (per power rail color coding: **Partial IO RET** & **DDR RET**) while all other SoC supplies are disabled

B) Using the "Always On" VSYS_3V3 pre-reg VIO to supply SoC's VDDSHV_CANUART and enables "CANUART IO signal toggling" to wake-up the system.

C) Using configurable power resources (PMIC, Buck, LDO, Load switch) that can be disabled per power down seq to enter low power mode (reduced SoC power) and enabled per power up seq to exit from low power mode and return to full active SoC operations.

D) Using 1x I2C channel for SoC & PMIC communications that combines PMIC control & status with FuSa operations (i.e., servicing Watchdog Timer) that enables GPIO1 (n= nSLEEP) function) connection to SoC's PMIC_LPM_EN signal that commands PMIC to enter (low) & exit (high) low power RET modes.

E) Arming the PDN PFSM by SW I2C writes to set PMIC I2C_TRIGGER_* register bits that direct which RET mode to enter when PMIC_LMP_EN signal asserts low as follows:

I2C_TRIGGER_7	I2C_TRIGGER_5	PDN State
0	0	SoC remains in Full Active state
0	1	Enters "IO/Partial IO only RET" low power mode (same as J7xxx PDN-3x systems for SW compatibility)
1	0	SoC remains in Full Active state
1	1	Enters "IO/Partial IO + DDR RET" low power mode (same as J7xxx PDN-3x systems for SW compatibility)

PMIC's GPIO6 supports 2x PDN operations:

- A) **DISABLE_WDOG:** PMIC latches logic level at GPIO6 pin at PMIC's Wait4Enable state just before beginning a start-up sequence.
 - a) High level at GPIO6 pin (SW-1/Imp-1 = closed/installed) directs PMIC to enable Watch-Dog Timer (setting WD_PWRHOLD bit to disable timer's long-window time-out).
 - b) Low level at GPIO6 pin (due to discrete load current or LDO2 both having pull-downs to GND whenever disabled) directs PMIC to enable Watch-Dog Timer (setting WD_PWRHOLD bit to enable timer's long-window time-out).
- B) **Safety-Error:** During power up seq, PMIC's PFSM sets GPIO6 = Error Signal Monitor (ESM) function to enable PMIC to capture SOC SAFETY_ERROR pulses.
 - a) EVM's default configuration is to connect SOC MCU_ERRORn signal to PMIC's GPIO6/ESM function.
 - b) An AND gate with inputs connected to SOC MCU & MAIN_SAFTY_ERRORn signals enables logical combination of both error signals for PMIC's GPIO6/ESM function.

The SOC's MAIN_ERROR signal is muxed behind Trace & CPWC interfaces that the EVM must support. Therefore, an in-line mux switch typically isolates the MAIN_ERROR net from the SOC and a dedicated enable MCU_ERROR signal to pass through the AND gate as default connection to PMIC's ESM function. If the EVM has a combined MCU & MAIN_ERROR signal, then reconfiguration of SOC's PINMUX settings to output MAIN_ERRORn and EVM mux switch to connect with the AND gate input will be required.

PMIC ext voltage monitoring (VMON) are needed for VDD_CORE & VDD_IO_3V3 rails supplied from discrete power devices for FuSa ASIL-B. NVM settings provide:

- A) Differential voltage monitoring is needed for VDD_CORE since supply is < 1.0V. So PMIC's diff VMON feature using VMON1_P input pin & GPIO3 = VMON1_M function are needed.
- B) Single-Ended VMON2 uses GPIO4 = VMON2 function for monitoring VDD_IO_3V3 since supply > 1.0V and a discrete load switch is used up to loads > 165mA.

1. PMIC's LDO2 Vout (3.3V) will be used as the control signal for the discrete load switch.
2. PMIC's GPIO4 = VMON2 function is needed to provide OV/UV VMON coverage for FuSa ASIL-B on output side of discrete load switch

PDN shows default option to supply SoC's VDDA_3P3_USB from the digital VDD_IO_3V3 rail with in-line supply filter to reduce switching noise to give "reasonable" USB 2.0 data eye performance for product development tasks. An option has been provisioned to supply VDDA_3P3_USB from a low noise LDO derived from a V5V5_5V input to give optimal USB 2.0 data eye performance if needed. If USB 2.0 I/F is not used, then the digital VDD_IO_3V3 rail can supply VDDA_3P3_USB directly without in-line analog filter.

1) PDN shows default option to supply SoC's VPP from a 400mA rated LDO (i.e. PNs: TPS745-Q1 & TPS7A21-Q1) with fast transient response, active pull-down on Vout and SoC GPIO signal for enable control. This configuration supports the capability for "in-the-field" Efuse programming updates to High Security (HS) SoCs. SoC devices come in two types: General Purpose (GP) & High Security (HS). All GP and pre-programmed HS devices can leave the VPP input supply unconnected per DM since no Efuse programming is needed.

3) PDN shows default option to supply SoC's fixed 0.85V inputs (VDDR_CORE, VDD_MMC0, VDDA_OP085_xxx) from an independent Buck via VDD_RAM_0V85 rail which allows VDD_CORE rail to operate at 0.75V for reduced power. An option to supply all SoC low voltage core processing supplies (< 1.1V) from a common 0.85V VDD_CORE power rail to reduce PDN BOM cost has been provisioned for future testing if needed.

5) PDN shows default option to supply SoC's VDDA_OSC/PLL/TEMP/MCU & VDDA_1P8_CSIDSI/OLDI/SERDES/USB input supply groups from 2x independent PMIC LDOs via VDA_PLL_1V8 & VDA_PHY_1V8 power rails to avoid possible high-speed PHY switching transient impacts to OSC/PLL/TEMP/MCU supplies/SoC clocking. An option to supply all SoC 1.8V analog supplies from a common 1.8V PMIC LDO/power rail has been provisioned for future test to min BOM cost & PCB area by enabling PDN/PMIC resource optimizations.

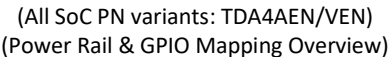
	VSEL connection	Default output voltage	QC device address	Droop compensation	Transient non-sync mode
	VSEL 6.2k to GND	0.85V	0x44	enabled	enabled
	VSEL shorted to GND:	0.75V	0x45		
	VSEL shorted to VIN:	0.875V	0x46		
	VSEL with 47k to VIN:	0.8V	0x47		

1. SoC's 4x A53s clock at **1.4GHz** with **SERDES operational per "EVM" use cases**
(EVM UC combines FCD + CMS use cases)
2. Functional Safety: **ASIL-B** capable system
3. SDRAM: 1x EMIF with LPDDR4 (32Gb, 4x Die, 32b, 4000MTs, VIO = 1.1V)
4. Flash: Octal SPI or NOR-Flash for boot & eMMC for mass storage
5. Dual Voltage Signaling: Dual VIO (3.3/1.8V)
6. Low power modes:
 - a. **Partial IO Retention**
 - b. **Partial IO + DDR Retention**

- **Summary ASIL-B system requirements:**
 1. A safety monitoring processor independent from SoC
 2. OV monitoring & protection on SoC system's input voltage
 3. OV & UV monitoring on all "safety critical" SoC power rails
 4. Watchdog (WD) monitoring of safety processor
 5. Independent WDM comm channel with interrupt to safety proc
 6. Safety processor error monitoring & reset capabilities
 7. Error indicator signal for external safety critical systems
- **Additional system requirements for ASIL-C & D:**

(Same as ASIL-B plus items below)

 8. Over current monitoring on all "safety critical" SoC power rails
 9. SoC Main processor error monitoring & reset capabilities



- a. Compliant high-speed UHS-I SD Card
- b. Best Effort USB 2.0 data eye (analog filter VDD_IO_3V3 to reduce noise for better eye)
- c. HS SoC Efuse programming on-board (needs 1 indep pwr rail & 1 cntrl signal)

V0.22	10/10/2023	BMc	1. Updated Single Bit Dual Supply Tri-State buffer PN interfaced to PMIC's GPIO6 per SCH
V0.23	12/8/23 01/10/24	BMc	1. Added power mapping R-Muxes labels (PM-#) to identify population options for alternative power maps supported by SoC 2. Updated Pwr-Mux (PM) resistor Ref Des #s to align with released vE1 assignments

